

Phase-locked Loop with Analog Phase Rotator

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5 BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to high speed semiconductor integrated circuits. In particular, the present invention relates to integrated circuits including  
10 phase-locked loops used in high speed applications.

SUMMARY OF THE INVENTION

The present invention provides a phase-locked loop and its associated methods. In one embodiment, a phase detector receives an input signal and a first internal periodic  
15 signal and provides a phase signal indicative of a phase difference between the input signal and the internal signal. A rotator then receives the phase signal and provides a first and second periodic signals each having a period which is a function of the phase difference, the first and the  
20 second periodic signals being 90 degrees out of phase with each other. An interpolator circuit then linearly combines the first and second periodic signals with a third periodic signal and a fourth periodic signal to provide the first internal periodic signal.

25 In one embodiment, the interpolator circuit further provides a second internal periodic signal, the second internal periodic signal being 90 degrees out of phase relative to the first internal periodic signal. The phase-locked loop may further include a low-pass filter provided  
30 between the phase detector and the rotator.

In one embodiment, the rotator in the phase-locked loop provides that the first ( $Q$ ) and second ( $I$ ) periodic signals are given by the equations:

$$Q = A \cos(kf(p))$$

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$$I = A \sin(kf(p))$$

where  $A$  is the amplitude of the  $Q$  and  $I$  signals,  $k$  is a gain of the rotator circuit, and  $f(p)$  representing a function of the phase difference. In one instance, the phase difference is represented in the phase signal as a voltage. The third and fourth periodic signals may each have a frequency that is substantially a frequency of the input signal. The rotator may further include an enforcer providing an error signal indicating a deviation in amplitude the first and second periodic signals. This error signal is fed back to the rotator to maintain a substantially constant amplitude in the  $Q$  and  $I$  signals. In one instance, the error signal is a function of the value  $\Delta = r^2 - I^2 - Q^2$ , where  $r$  is a desired amplitude for the  $Q$  and  $I$  signals. In one implementation, the desired amplitude is approximately 0.4 volts.

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In one embodiment, the phase-locked loop of the present invention is provided with third ( $x$ ) and fourth ( $y$ ) periodic signals given by the equations:

$$x = \sin \omega t ,$$

$$y = \cos \omega t ,$$

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where  $\omega$  represents a frequency of the third and fourth periodic signals.

In one embodiment, the first internal periodic signal  $S(t)$  is given by:

$$S(t) = \sin(\omega t - \phi) ,$$

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where  $\phi$  is indicative of said phase difference.

The present invention is better understood upon consideration of the detailed description below and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

5        Figure 1 is a block diagram of a phase-locked loop 100, in accordance with one embodiment of the present invention.

Figure 2 shows one implementation of phase-locked loop 100 in phase-locked loop circuit 200.

10       Figure 3 is a block diagram showing rotator 103, according to one embodiment of the present invention.

Figure 4 shows rotator circuit 800, which can be used to implement rotator 103, in accordance with the embodiment of the present invention shown in Figure 3.

15       Figure 5 shows differential multiplier circuit 900, which can be used to implement any of multipliers 701-704 of Figure 4.

Figure 6 shows integrator circuit 1000, which can be used to implement either one of integrators 705-706.

20       Figure 7 shows enforcer circuit 1100, which can be used to implement enforcer 707 of Figure 3, in accordance with one embodiment of the present invention.

Figure 8 shows interpolator circuit 1200, which can be used to implement interpolator 210 of Figure 2, in accordance with one embodiment of the present invention.

25       Figure 9 shows differential amplifier circuit 1300, which can be used to implement either one of differential amplifiers 1210 and 1211 of Figure 8.

30       Figure 10 shows interpolator circuit 1400, which can be used to implement either one of interpolator circuits 1212 and 1213.

Figure 11 shows multiplier circuit 1500, which can be used to implement either of multiplier circuits 1401 and 1402 of Figure 10.

To facilitate comparisons among the figures and to avoid repetition, like elements in the figures are accorded like reference numerals.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention provides a phase-locked loop circuit and a method for providing such a phase-locked loop circuit.

Figure 1 is a block diagram of a phase-locked loop 100, in accordance with one embodiment of the present invention. As shown in Figure 1, phase detector 101 receives differential data signal 110 and output differential signal 115 to provide phase signals 111. The voltage difference between phase signals 111 (i.e., voltage difference  $v(t)$  between the component signal "up" or 111a and "down" or 111b of phase signals 111) represents a measure of the phase difference between data signal 110 and output signal 115. Phase signals 111 are provided to low-pass filter 102. Low-pass filter 102 provides filtered differential signal 112 to rotator 103. In response, rotator 103 provides two differential phase signals 113 and 114, also referred to as differential phase signals  $I(t)$  and  $Q(t)$  below, according to equations (1) and (2):

$$Q = A \cos(k \int v(t) dt) = A \cos k\phi \quad (1)$$

$$I = A \sin(k \int v(t) dt) = A \sin k\phi \quad (2)$$

where  $A$  is the amplitude of the  $Q$  and  $I$  signals,  $k$  is a gain in rotator 103, and  $\phi$  represents the phase difference between clock signal 110 and output signal 115, integrated over a specified time period.

Interpolator 104 receives differential phase signals 113 and 114 and differential quadrature signals 116 and 117 (respectively denoted by  $\sin \omega t$  and  $\cos \omega t$ , where  $\omega$  is the clock frequency of data signal 110) to provide output  
5 differential quadrature signal 115 (denoted as  $C(t)$  below), according to equation (3):

$$C(t) = A \cos \omega t \cos k\phi + A \sin \omega t \sin k\phi = A \cos(\omega t - k\phi) \quad (3)$$

Quadrature signals 116 and 117 are internal clock signals derived from the output signals of an internal clock  
10 generator (not shown). Optionally, output differential quadrature signal 118 (denoted as  $S(t)$ , not shown in Figure 1), which is 90 degrees out of phase with signal  $C(t)$ , can also be provided in accordance with equation (4):

$$S(t) = A \sin \omega t \cos k\phi - A \cos \omega t \sin k\phi = A \sin(\omega t - k\phi) \quad (4)$$

15 Output signal 115 and, optionally output signal 118, can then be provided to vary the phase of various internal clock signals, so as to maintain phase relationships with respect to input data signal 110. Output signal 115 can be provided to phase detector 101, as shown in Figure 1.  
20 Phase-locked loop 100 tends to minimize the phase difference  $\phi$  between input clock signal 110 and output signal 115.

One implementation of phase-locked loop 100 is shown in Figure 2 as phase-locked loop circuit 200. In phase-locked loop circuit 200, a conventional clock generator (not shown)  
25 provides internal quadrature clock signals 116 and 117, collectively referred to as clock signals 207, at approximately 1.6 GHz. At the same time, phase detector 101 receives input data signal 110, and output signals 115 and 118, and provides "up" and "down" phase signals 111 (i.e., signals 111a and 111b). Phase detector 101 can be  
30 implemented, for example, by a conventional "bang-bang" detector (also known as an "Alexander's phase detector").

In Figure 2, phase signals 111a and 111b of phase detector 101 are provided to low-pass filter 102. Low-pass filter 102 can be implemented, for example, by a conventional low-pass filter circuit. Figure 2 shows that integrated phase signals 112a and 112b are provided to rotator 103. Figure 3 is a block diagram showing rotator 103, in accordance with one embodiment of the present invention. As shown in Figure 3, rotator 103 includes multipliers 701-704, integrators 705-706 and enforcer 707.

In rotator 103, multiplier 701 multiplies differential phase signal 112 (i.e., signal  $v(t)$ ) with differential signal 114 (i.e., quadrature signal  $Q(t)$ ) to provide differential signal 710, which is provided to integrator 705. Integrator 705 integrates the sum of differential signal 710 and differential output signal 711 to provide differential signal 113 (i.e., quadrature signal  $I(t)$ ). Similarly, multiplier 702 multiplies the polarity-reversed differential phase signal 112 (i.e., signal  $-v(t)$ ) with differential signal 113 (i.e., quadrature signal  $I(t)$ ) to provide differential signal 712, which is provided to integrator 706. Integrator 706 integrates the sum of differential signal 712 and differential output signal 713 to provide differential signal 114 (i.e., quadrature signal  $Q(t)$ ). Differential signals 711 and 713 are the product of output differential signals 708 (" $\Delta$ ") and 113, and the product of differential signals 708 and 114, respectively. Differential signal 708 is defined by the following equation (5):

$$\Delta = r^2 - I^2 - Q^2 \quad (5)$$

where  $r$  is a desired amplitude for signals  $I$  and  $Q$ . Thus, the values of  $I(t)$  and  $Q(t)$  are governed by the following equations (6) and (7):

$$I(t) = \int (k_1 k_2 Q(t) v(t) + k_3 \Delta \cdot I(t)) dt \quad (6)$$

$$Q(t) = \int (-k_1 k_2 I(t) v(t) + k_3 \Delta \cdot Q(t)) dt \quad (7)$$

where  $k_1$  and  $k_2$  are the gains of each of multipliers 701-704 and each of integrators 705-706, and  $k_3$  is the total path gain in enforcer 707. Since  $\Delta$  is constant over the relevant time period of integration (i.e., over half a period of clock signal 116 or 117), the resulting quadrature signals 113 and 114 are given by equations (8) and (9):

$$I(t) = I_0 e^{k_3 \Delta t} \sin k \int v(t) dt \quad (8)$$

$$Q(t) = Q_0 e^{k_3 \Delta t} \cos k \int v(t) dt \quad (9)$$

where  $I_0$  and  $Q_0$  are initial values for the  $I(t)$  and  $Q(t)$  signals, and  $k$  is the product  $k_1 k_2$  provided above. Because  $\Delta$  is an error signal representing the transient amplitude deviation from the trigonometrical identity relating  $I(t)$  and  $Q(t)$ , and since the solutions of  $I(t)$  and  $Q(t)$  as provided above in equations (8) and (9) enforces the trigonometrical identity, the value of  $\Delta$  tends to zero, resulting in:

$$I(t) = R_0 \sin k \int v(t) dt \quad (8)$$

$$Q(t) = R_0 \cos k \int v(t) dt \quad (9)$$

where  $R_0$  is the steady state amplitude of signals  $I(t)$  and  $Q(t)$ .

Figure 4 shows rotator circuit 800, which can be used to implement rotator 103, in accordance with the embodiment of the present invention shown in Figure 3 above. The operation of rotator circuit 800 is substantially the same as that described above with respect to Figure 3 above. A detailed description of the operation of rotator circuit 800 is therefore omitted. In rotator circuit 800, a voltage generator (not shown) provides a bias voltage  $V_{CM-REF}$  to integrators 705 and 706. Such a voltage generator can be implemented by serially connected diodes between supply voltage  $V_{CC}$  and the ground reference, with  $V_{CMREF}$  provided

from the output terminal of the diode connected to  $V_{CC}$ , thus providing  $V_{CMREF}$  to be approximately  $\frac{3}{4} V_{CC}$ , when four serially connected diodes are used.

Figure 5 shows differential multiplier circuit 900, which can be used to implement any of multipliers 701-704 of Figure 4. As shown in Figure 5, differential multiplier circuit 900 includes differential amplifier 950 and multiplier 951. Differential amplifier 950 provides an output differential signal on terminals 906 and 907 to multiplier 951. In differential amplifier 950, a bias voltage is provided at terminal 903 to set the current sources represented by NMOS transistors 928-930. Diode-connected PMOS transistors 936 and NMOS transistor 930 together provide a first bias voltage, which is applied to the gate terminals of cascode PMOS transistors 920 and 921. Similarly, diode-connected PMOS transistor 935 and NMOS transistor provides a second bias voltage, which is applied to PMOS transistors 937 and 938. Together, PMOS transistors 920-921 and 937-938 set a DC offset voltage for the output signals of differential amplifier 950 at terminals 906 and 907. The first input differential signal at terminals 901 and 902, i.e., the signals at the gate terminals of input transistors 922 and 923, respectively, are amplified to a proportional AC voltage superimposed on the DC offset voltage at output terminals 906 and 907.

The signals of output terminals 906 and 907 set the current sources in multiplier 951 represented by NMOS transistors 933 and 934. Since the second input signal at input terminals 904 and 905 are provided to the gate terminals of input transistors 924-927 of multiplier 951, the differential signal at terminals 908 and 909 represents the product of the first and second input differential signals. In this embodiment, both the input and output signals of differential multiplier circuit 900 are expected to have a DC offset voltage of 1.35 volts, and an AC



component varying within 0.2 volts about the DC offset voltage.

Figure 6 shows integrator circuit 1000, which can be used to implement either one of integrators 705-706. As shown in Figure 6, bias circuit generator 1050 provides a bias voltage at terminal 1034 that is applied to each of the current sources represented by transistors 1013-1035. The bias voltage is provided by the current in the current path including PMOS transistor 1009, NMOS transistor 1012, and resistors 1011. This bias voltage is approximately three diode-drops from supply voltage  $V_{CC}$ , being substantially the voltage drop across the source and drain terminals of PMOS transistors 1009 and 1005, and the gate-to-source voltage of PMOS transistor 1006. At the same time, PMOS transistor 1023 and NMOS transistor 1013 provides a second bias voltage for biasing PMOS transistors 1018 and 1019. The input differential signal across terminals 1032 and 1033, applied to the gate terminals of transistors 1016 and 1017, are amplified and provided as an output differential signal at output terminals 1030 and 1031. Output terminals 1030 and 1031 are connected to MOS capacitors 1001-1002 and 1003-1004, respectively. The output signals at terminals 1030 and 1031 have a DC offset voltage set by the  $V_{CM-REF}$  bias voltage discussed above, as a result of the action of NMOS transistors 1020-1022, which receive the signals at terminal 1030, 1036 and 1031, respectively.

Figure 7 shows enforcer circuit 1100, which can be used to implement enforcer 707 of Figure 8, in accordance with one embodiment of the present invention. As shown in Figure 7, enforcer circuit 1100 includes differential multipliers 1101-1103, and resistors 1104-1107 and NMOS transistor 1108. Differential multipliers 1101-1103 can each be implemented, for example, by differential multiplier circuit 900 of Figure 5. Multipliers 1101 and 1102 are configured to compute the squares of signals 113 and 114 (i.e.,  $I^2(t)$  and  $Q^2(t)$ ), respectively. Transistor 1108 is biased by input

bias signal at terminal 1120. In conjunction with resistors 1104-1105, transistor 1108 provides a current that is approximately 200 uA, thus providing a 0.4 volts differential input signal to multiplier 1103. 0.4 volts correspond to approximately twice the peak amplitude of the AC components of input signals 113 and 114. The output terminals of multipliers 1101-1103 are configured to provide output differential signal 708, which is the output differential signal of multiplier 1103, less the sum of the output differential signals of multipliers 1101-1102. (The polarity of the output differential signal of multiplier 1101 and 1102 are reversed.) Thus, output differential signal 708 (i.e., signal  $\Delta$ ) represents the value  $\Delta = r^2 - I^2 - Q^2$ .

Returning to Figure 2, differential signals 113 and 114 and differential clock signals 116 and 117 are provided to interpolator 210 to provide differential output signals 115 and 118. Figure 8 shows interpolator circuit 1200, which can be used to implement interpolator 210 of Figure 2, in accordance with one embodiment of the present invention. As shown in Figure 8, interpolator circuit 1200 includes amplifier circuits 1210 and 1211, and interpolator circuits 1212 and 1213. As configured in interpolator circuit 1200, interpolator circuits 1212 and 1213 each combine linearly phase signals 1201 (i.e., amplified phase signal 113 or  $I(t)$ ) and 1202 (i.e., amplified phase signal 114 or  $Q(t)$ ) with quadrature signals 116 ( $\sin \omega t$ ) and 117 ( $\cos \omega t$ ) to provide output differential signals 115 ( $C(t)$ ) and 118 ( $S(t)$ ), respectively.

Figure 9 shows differential amplifier circuit 1300, which can be used to implement either one of differential amplifiers 1210 and 1211. As shown in Figure 9, differential amplifier 1300 provides an output differential signal on terminals 1306 and 1307. In differential amplifier 1300, a bias voltage is provided at terminal 1303 to set the current sources represented by NMOS transistors

1328-1330. Diode-connected PMOS transistors 1336 and NMOS transistor 1330 together provide a first bias voltage, which is applied to the gate terminals of cascode PMOS transistors 1320 and 1321. Similarly, diode-connected PMOS transistor 1335 and NMOS transistor provides a second bias voltage, which is applied to PMOS transistors 1337 and 1338. Together, PMOS transistors 1320-1321 and 1337-1338 set a DC offset voltage for the output signals of differential amplifier circuit 1300 at terminals 1306 and 1307. The first input differential signal at terminals 1301 and 1302, i.e., the signals at the gate terminals of input transistors 1322 and 1323, respectively, are amplified to a proportional AC voltage superimposed on the DC offset voltage at output terminals 1306 and 1307.

Figure 10 shows interpolator circuit 1400, which can be used to implement either one of interpolator circuits 1212 and 1213. As shown in Figure 10, interpolator circuit 1400 includes multiplier circuits 1401 and 1402, each multiplier circuit being provided to multiply an amplified phase signal (i.e., signal 1410 or 1415) with a quadrature signal (i.e., signal 1411 or 1416). The differential output signals of multiplier circuits 1401 and 1402 are summed at terminals 1412, which is suitably amplified by amplifier 1403 to provide output differential signal 1413.

Figure 11 shows multiplier circuit 1500, which can be used to implement either of multiplier circuits 1401 and 1402 of Figure 10. As shown in Figure 11, in multiplier circuit 1500, the signals of input terminals 1503 and 1504 set the current sources represented by NMOS transistors 1510 and 1511. Since the second input signal at input terminals 1501 and 1502 are provided to the gate terminals of input transistors 1512-1515 of multiplier 1500, the differential signal at terminals 1505 and 1506 represents the product of the first and second input differential signals.

The above detailed description is provided to illustrate specific embodiments of the present invention. Numerous modifications and variations within the scope of the present invention are possible. The present invention

5 is set forth in the following claims.